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Westinghouse

ELECTRIC CORPORATION

MICROMINIATURE INTEGRATED CIRCUIT PACKAGE

Unclassified Final Report

Signal Corps Contract No. DA-36-039-SC-90850

DA Project No. 3A99-21-002-01

Final Report

July 1, 1962 to August 1, 1963

Prepared for
U.S. Army Signal Research and Development Laboratory
Fort Monmouth, New Jersey

WESTINGHOUSE ELECTRIC CORPORATION

Molecular Electronics Division

Elkridge Maryland

MICROMINIATURE INTEGRATED CIRCUIT PACKAGE

Unclassified Final Report

Signal Corps Contract No. DA-36-039-SC-90850

SCTR SCL-7643, October 17, 1961

DA Project No. 3A99-21-002-01

FINAL REPORT

July 1, 1962 to August 1, 1963

OBJECT

Development work directed toward development and production of hermetic planar packages for semiconductor devices in accordance with contract requirements.

REPORT PREPARED BY:

E. P. Barbaro

WESTINGHOUSE ELECTRIC CORPORATION

Molecular Electronics Division

Elkridge Maryland

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PURPOSE

The purpose of this investigation is to develop a .225 inch square planar, hermetic, integrated circuit package for mounting on .310 inch square micro-module wafers. The packages were to be developed to contain integrated circuits of the type specified in paragraph 1.2 of Technical Requirements SCL-7643. The packages are to be constructed from compatible glass materials.

A minimum of twelve leads, three on each side of the .225 inch square package, will be provided. A circuit mounting area of .120 inch square will be available within the enclosure. The height of the package may be adjusted up to .090 inches maximum.

After initial approval of mechanical samples, devices are to be assembled to demonstrate package feasibility. On approval of packaged assemblies and environmental evaluation of sealed mechanical samples by the Signal Corps, production of 10,000 packages are required to prove production capability.

ABSTRACT

Design and fabrication of two metal to glass seal microminiature integrated circuit packages were completed. One which utilized the .310 inch square ceramic base as an integral portion of the package and the other a .225 inch square package per the stated requirements of the contract. The .310 inch square package required more development as leak rates of only $< 1 \times 10^{-6}$ cc/sec at one atmosphere were achieved. However, on the contract package lead rates $< 1 \times 10^{-8}$ cc/sec at one atmosphere were attained. This was accomplished through revisions of graphite molds, glass preform designs, kovar oxide layer control and sealing techniques.

To prove package feasibility, twenty-four ~~Westinghouse~~ functional electronic blocks were encapsulated in the .225 inch square microminiature planar package. No problems in assembly were encountered.

After approval of mechanical samples and packages with integrated circuits, production of the required 10,000 packages commenced. Environmental studies were conducted on this package type confirming reliability of the package structure. Application data was compiled for circuit mounting, wiring, sealing and hermeticity testing of the microminiature circuit package developed for this contract.

CONFERENCES

I. DATE: July 3, 1962

PLACE: Westinghouse Electric Corporation
Molecular Electronics Division
Youngwood, Pennsylvania

IN ATTENDANCE: Messrs. M. Robert Miller, U.S.A.S.R.D.L.
Kenneth G. Cooley, Westinghouse M.E.D.
Chester B. Wiszowaty, Westinghouse M.E.D.
E. P. Barbaro, Westinghouse M.E.D.

SUBJECT: 1. The objectives and scope of contract were completely reviewed.

2. An integral package for micromodule program was discussed.

II. DATE: October 12, 1962

PLACE: Westinghouse Electric Corporation
Molecular Electronics Division
Youngwood, Pennsylvania

IN ATTENDANCE: Dr. Gene Hohman, U.S.A.S.R.D.L.
Messrs. K. G. Cooley, Westinghouse M.E.D.
A. P. Kruper, Westinghouse M.E.D.
M. S. Saunders, Westinghouse M.E.D.
E. P. Barbaro, Westinghouse M.E.D.

SUBJECT: 1. The progress on package fabrication was discussed.

2. Environmental evaluation of 200 samples with devices was discussed.

3. The possible substitution of integrated circuits for the mesa transistors specified for encapsulation was reviewed.

CONFERENCES (Contd.)

III. DATE: November 26, 1962

PLACE: Fort Monmouth, New Jersey

IN ATTENDANCE: Messrs. M. Robert Miller, U.S.A.S.R.D.L.
E. P. Barbaro, Westinghouse M.E.D.

SUBJECT: 1. Discussed the status of package evaluation.

2. Reviewed the rejection of the draft of the First Quarterly Report. Rejection was due to omission of integral micromodule package work and technical report form.

IV. DATE: December 12, 1962

PLACE: Westinghouse Electric Corporation
Molecular Electronics Division
Youngwood, Pennsylvania

IN ATTENDANCE: Messrs. O. Pitzales, U.S.A.S.R.D.L.
K. G. Cooley, Westinghouse M.E.D.
M. S. Saunders, Westinghouse M.E.D.
A. P. Kruper, Westinghouse M.E.D.
J. D. Husher, Westinghouse M.E.D.
W. Williams, Westinghouse M.E.D.
J. M. Clayton, Westinghouse M.E.D.
T. L. Charland, Westinghouse M.E.D.

SUBJECT: 1. Evaluation of one hundred (100) packages already shipped.

2. Return of First Quarterly Report.

3. Discussion of number and type of integrated circuits to be packaged.

4. Extension of December 31, 1962, shipping date of delivery of 200 packaged devices.

CONFERENCES (Contd.)

V. DATE: April 11, 1963

PLACE: Westinghouse Electric Corporation
Molecular Electronics Division
Youngwood, Pennsylvania

IN ATTENDANCE: Dr. James Meindel, U.S.A.S.R.D.L.
Dr. E. A. Sack, Westinghouse M.E.D.
Messrs. J. D. Husher, Westinghouse M.E.D.
K. Dussinger, Westinghouse M.E.D.
E. P. Barbaro, Westinghouse M.E.D.

SUBJECT: 1. The progress of the package contract was discussed.

2. Additional contract program to cover an integral base circuit package.

MICROMINIATURE INTEGRATED CIRCUIT PACKAGE

Final Report

July 1, 1962 to August 1, 1963

Contract No. DA-36-039-SC-90850

I. INTRODUCTION

A package which was flat, hermetic and suitable for encapsulating microminiature integrated circuits and meet the requirements of subject contract was required. The package was to be composed of glass, ceramic, metals or any combination thereof, and the assembled microminiature integrated circuit which is composed of silicon should meet the electrical, mechanical and heat properties as set forth in Technical Requirements SCL-7643.

A drawing of such a package is shown in Exhibit 1. A maximum of twelve (12) kovar leads, three (3) on each edge on .050 inch centers of the .225 inch square package, is provided. A circuit mounting area of .120 inches square is available within the enclosure. The height of the package assembly including ceramic substrate is to be less than .090 inches. Final closure of the package can be accomplished by means of a ceramic or glass sealed kovar lid. Such a package was designed and debugged through revisions in oxide layers, graphite molds, sealing techniques, glass preform and component design. A package which was environmentally sound was achieved. The package can be mounted on a .310 inch square micromodule wafer as shown in Exhibit 2. Package leads can be resistance welded to the metallized regions on the ceramic.

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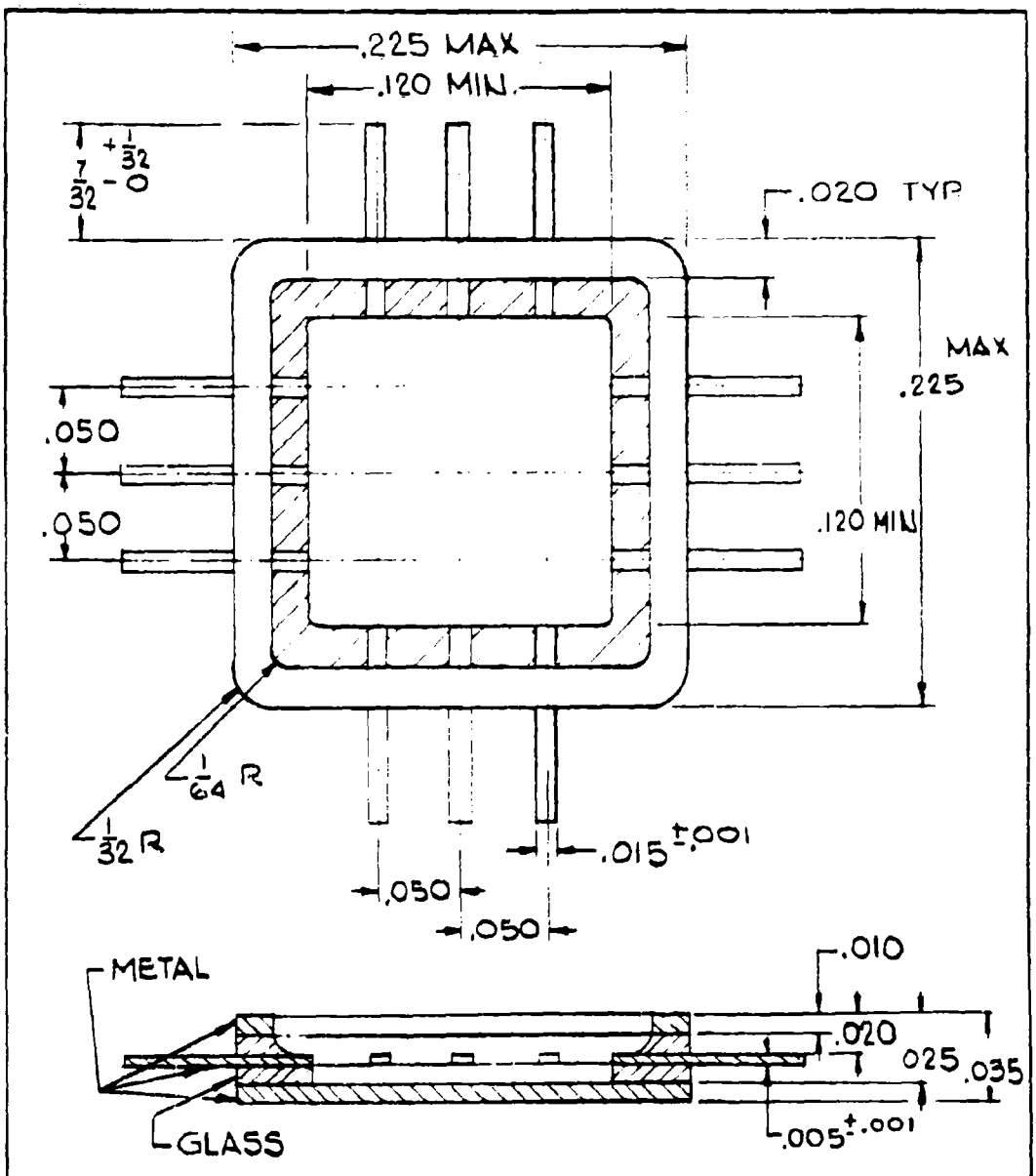
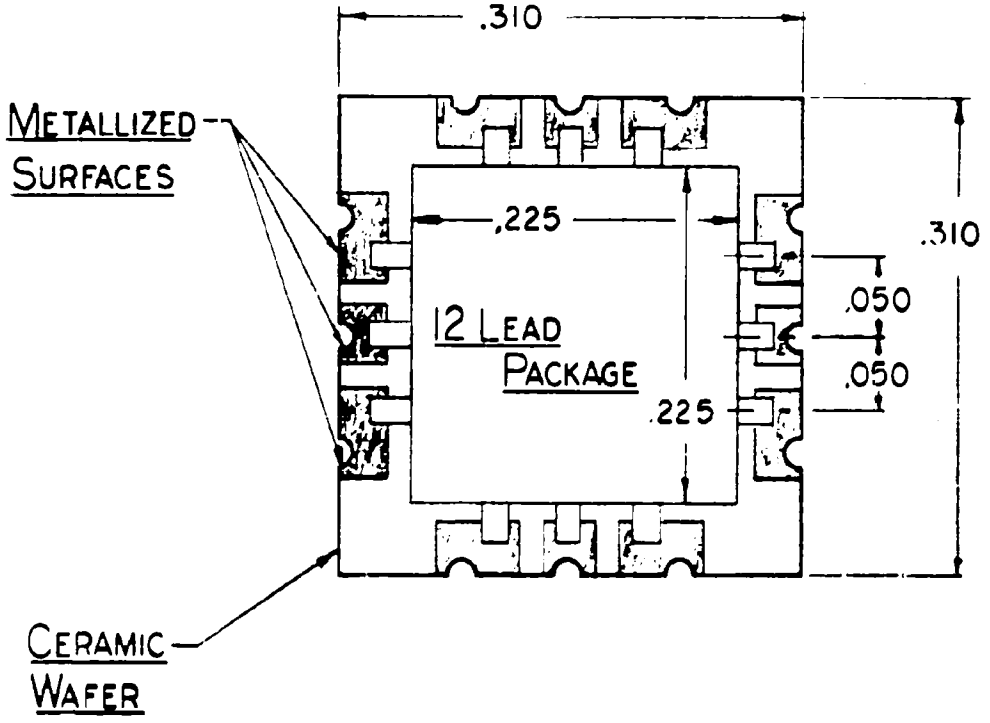


NOTE: ALL METAL PARTS TO BE PLATED WITH 70-150 x 10^{-6} INCHES OF GOLD

MICROMINIATURE CIRCUIT PACKAGE

EXHIBIT 1

WESTINGHOUSE ELECTRIC CORPORATION



PROPOSED 0.225 SQUARE PACKAGE
SUPERIMPOSED ON 0.310 SQUARE WAFER
FOR SIGNAL CORPS MICROMODULE

EXHIBIT NO.2

I. INTRODUCTION (contd.)

Twenty-four (24) Westinghouse Functional Electronic Blocks were assembled in the contract microminiature integrated circuit package. No major problems were encountered. Assembly was accomplished using standard transistor assembly equipment. These were forwarded to the Signal Corps for their evaluation. Also provided were ninety (90) sealed empty packages for mechanical and environmental evaluation by the Signal Corps.

A study of the hermeticity level was made. A comparison between Radiflo and helium leak test methods indicated that the contract package has a very high hermeticity level.

Application data was prepared for the encapsulation of the subject package. This covered processes from wafer bonding to hermeticity test of sealed packages. Environmental data on the microminiature integrated circuit package indicated it to be a sound structure.

A production run of 10,000 packages was made as the last sample requirements of the contract to indicate production feasibility. No major manufacturing problems were encountered. Yields were comparable to other Westinghouse Flat-Pak types; therefore, it would follow that the price structure would also be similar.

II. FACTUAL DATA

2.1 Package Design

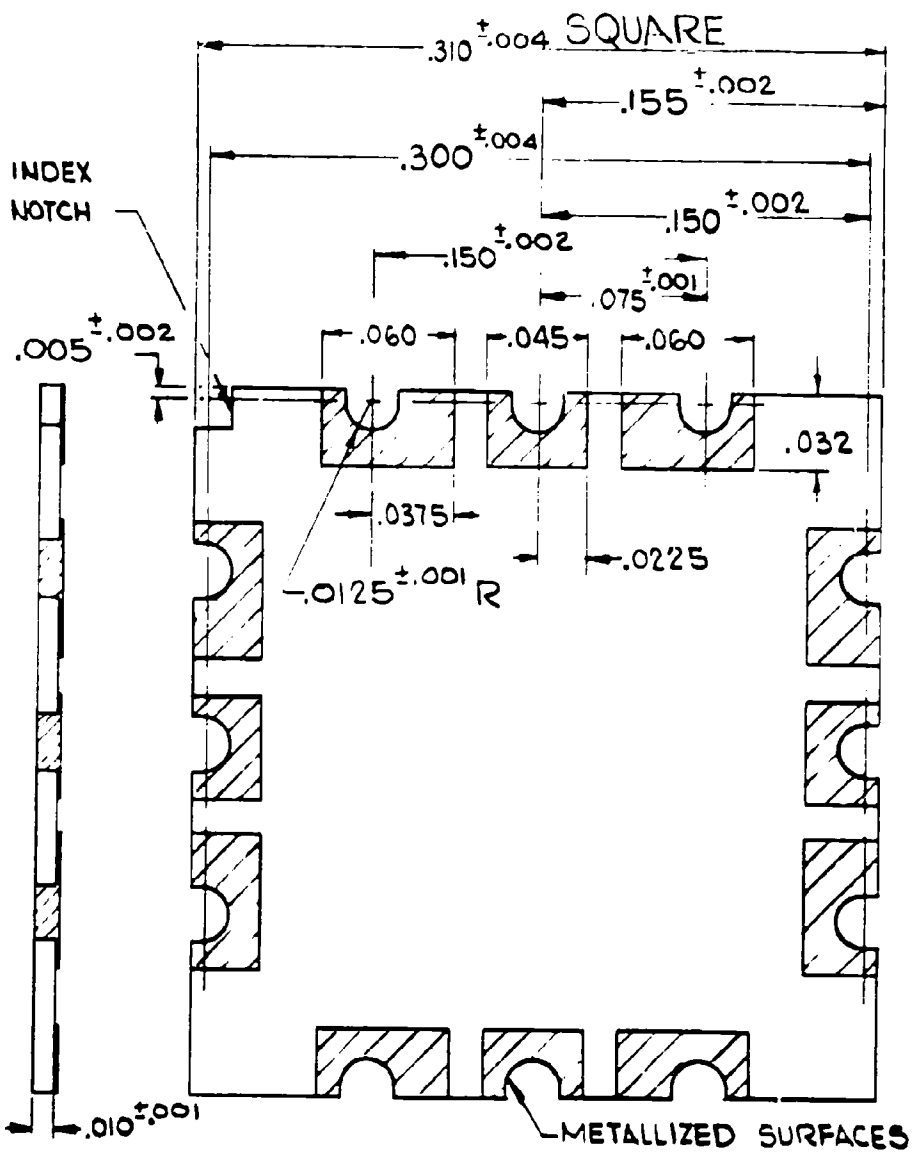
Two designs of microminiature integrated circuit packages were completed early in the program. A design which permits mounting to a .310 inch square ceramic was achieved. This package consisted

2.1 Package Design (contd.)

of a .220 inch square kovar base. Walls of a borosilicate are contained on the outer perimeter of the base. A kovar frame covers the top of the borosilicate glass to provide a metallic surface for lid attachment. Flat leads pass through the glass on .050 inch centers. All metal and glass parts are metallurgically bonded to form a hermetic and mechanically resistant package.

Inside the package there is a .120 inch square metal land for circuit mounting. All metal parts are gold plated to permit die bond, lead and lid attachment and provide an environmentally resistant package. See Exhibit 1 of microminiature integrated circuit package. A .310 inch square metallized wafer was designed to accept the .225 inch square microcircuit package. Lands are such that conventional .050 center leads of the microminiature integral circuit package can be welded to the ceramic metallized base. In this way circuitry can be interconnected by joining required lands on the micromodule wafers. See Drawing 2914848 for the metallized ceramic wafer and Figure 2 for the suggested mounting technique. A second design which was developed used the ceramic micromodule wafer as an integral part of the package. The intent of this design was to eliminate the necessity of welding or soldering package leads to the micromodule wafer. This package consisted of a .310 inch square metallized ceramic wafer .25 inch square x .025 glass preform and a .25 inch square x .010 metal frame. The glass preform is joined to the ceramic and the metal frame is hermetically sealed to the glass preform. This package design required no leads as the micromodule wafer is metallized with lands

WESTINGHOUSE ELECTRIC CORPORATION



MICROCIRCUIT PACKAGE WAFER

MATERIAL: METALLIZED SURFACES - "MOLLY MANGANESE" - .002 THICK, NICKEL PLATE .0001.
WAFER - "CERAMIC"

291A943

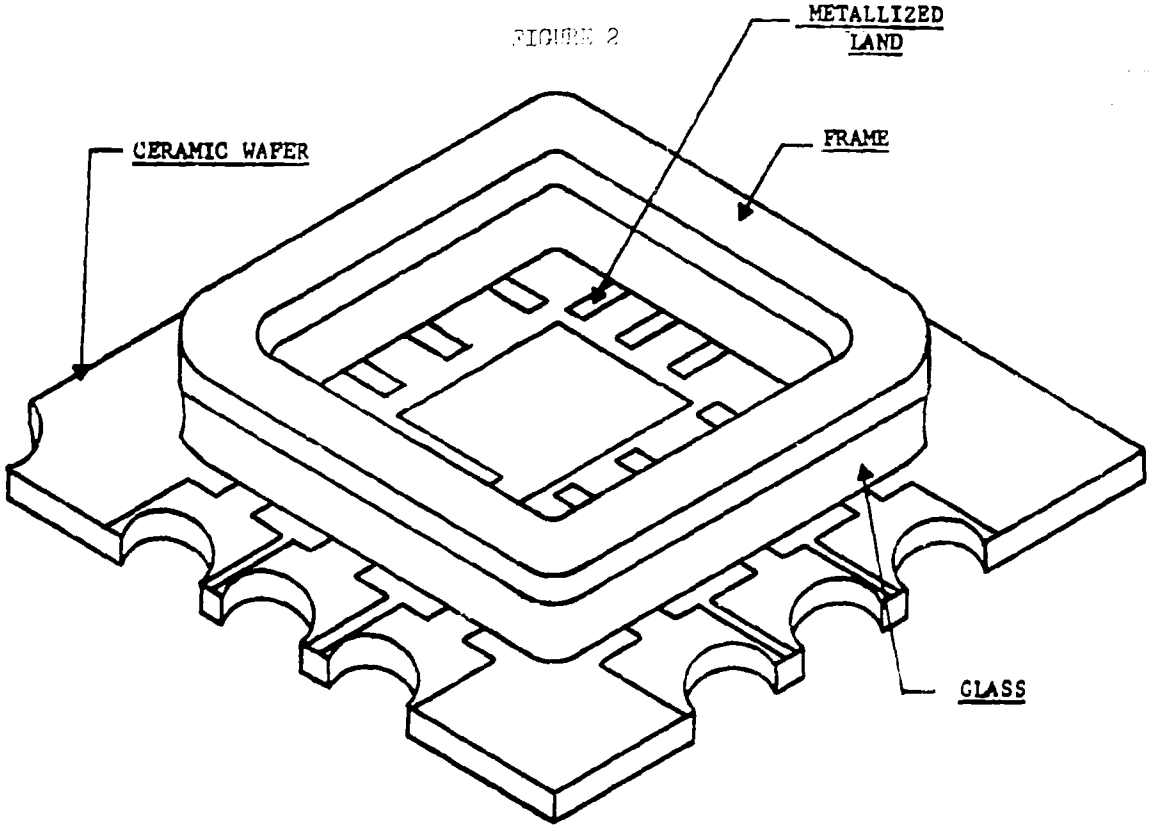


FIGURE 1 - INTEGRAL MICROMODULE PACKAGE

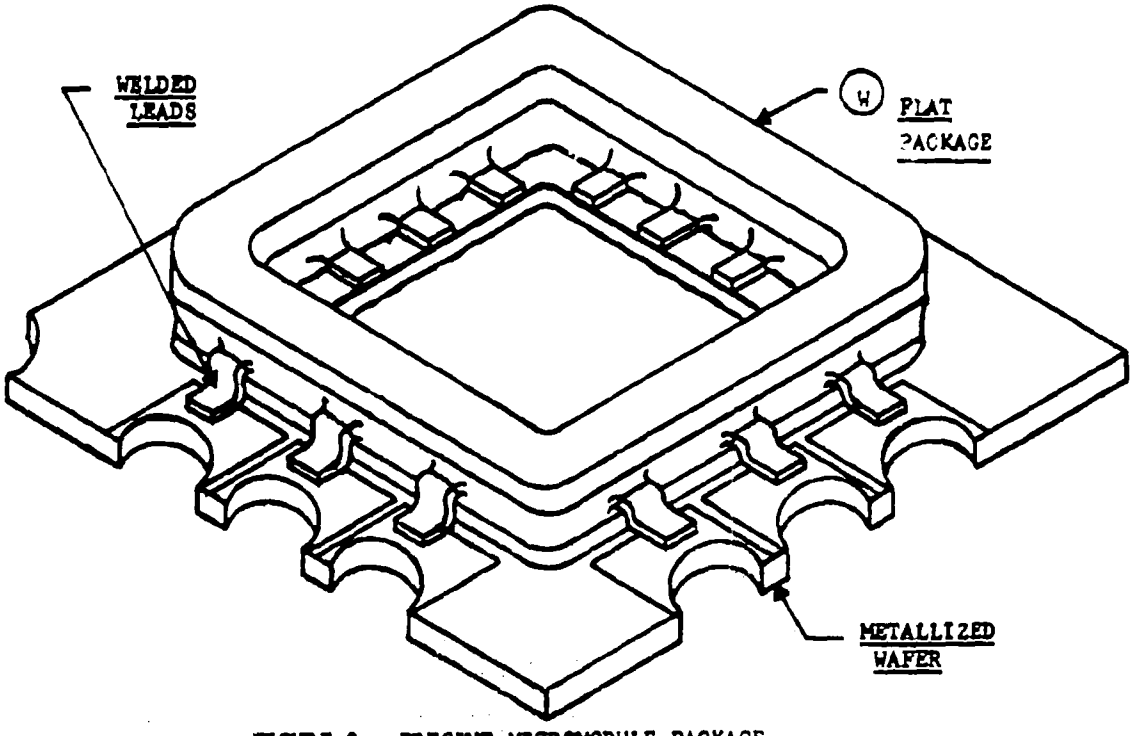


FIGURE 2 - PRESENT MICROMODULE PACKAGE

2.1 Package Design (contd.)

that provide a center bonding pad of .120 inches square and terminal bonding pads .020 x .015. These terminal pads extended to the micromodule notches on the periphery. See EDSK 291712 for micromodule wafer layout.

Also, see Figure 1 showing an isometric view of the integral base package. Sample packages were fabricated and evaluated by the Signal Corps. A problem of insufficient clearance between the .250 inch square frame and wafer periphery for assembly was the basic reason for rejection of this package type.

In a later proposal to the Signal Corps, a frame size of .225 inches square with a mounting area of .100 inches square was suggested. This package design would have real merit in that twelve less weld connections would exist per wafer resulting in increased reliability and reduced assembly cost.

2.2 Package Materials

The design and procurement of the component parts for manufacture of the microminiature integrated circuit package was completed. These parts are listed below with their respective drawing numbers.

Part	Drawing No.
Glass Preform - 7052 Glass	291A844
Kovar Frame	291A842
Kovar Lid and Bottom	291A845
Kovar Leads	1106A39H02

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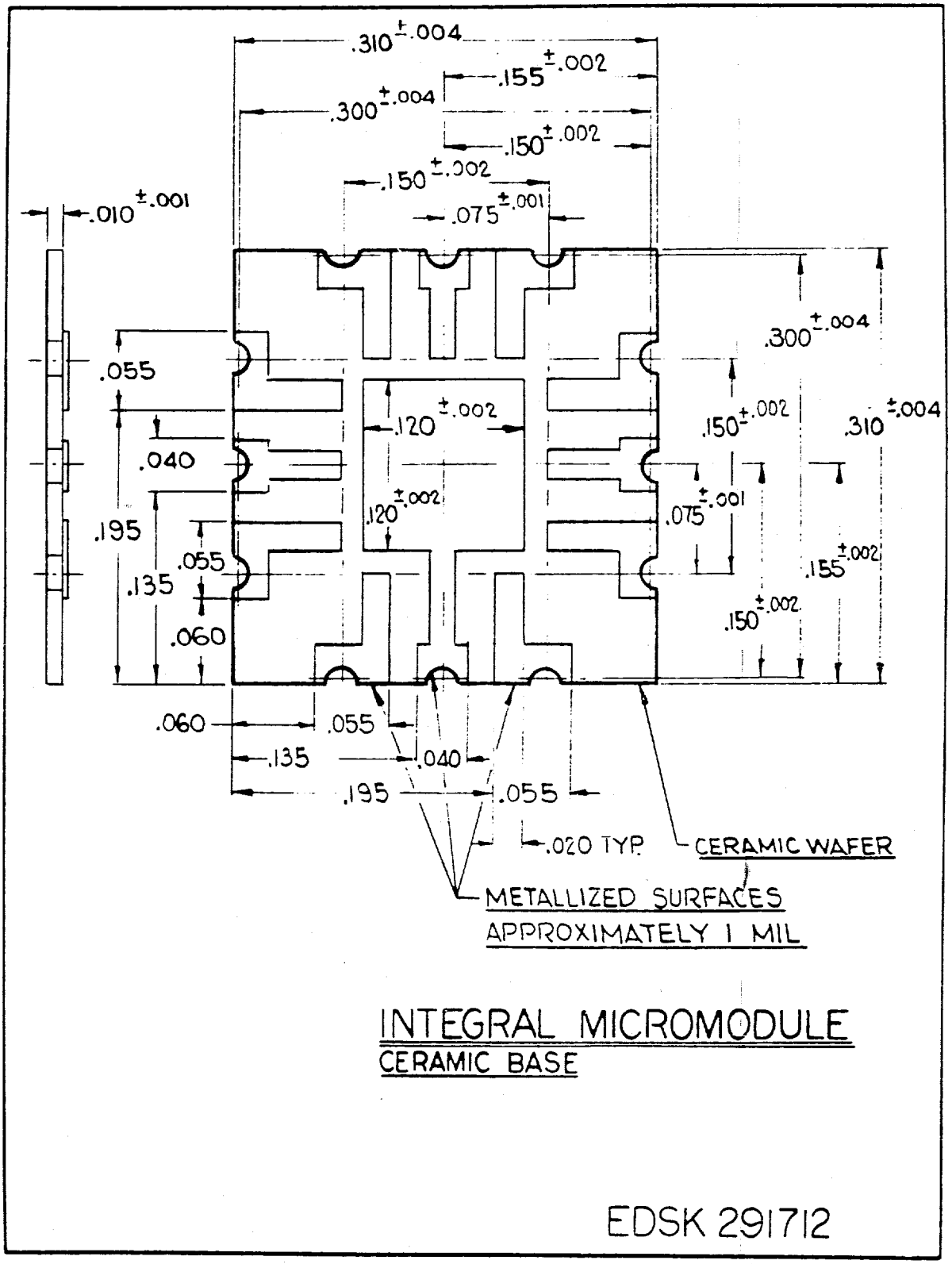
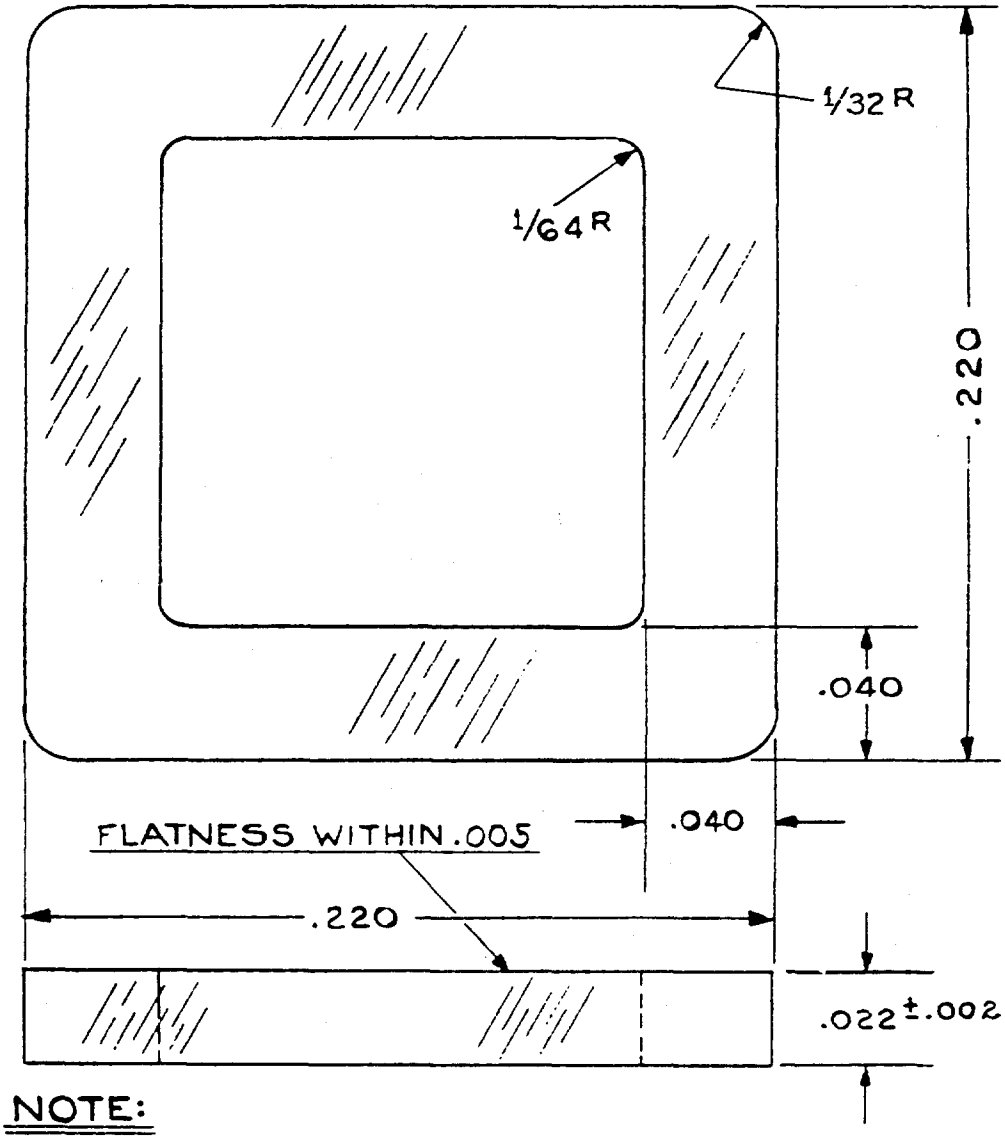


INTEGRAL MICROMODULE
CERAMIC BASE

EDSK 291712

S.O.	SUB.
D.	1

THICKNESS .022 WAS .030.
MATERIAL WAS 5072 BORON SILICATE GLASS.
D.Z. 3/22/63
EPB



NOTE:
ALL DECIMAL DIMENSIONS WITHIN .002 EXCEPT THICKNESS -.001.
MATERIAL - SURE SEAL RN GLASS.

STANDARD TOLERANCES UNLESS OTHERWISE SPECIFIED	
DECIMAL DIMENSIONS	±.005
FRACTIONS	±1/64
ANGLES	±1°

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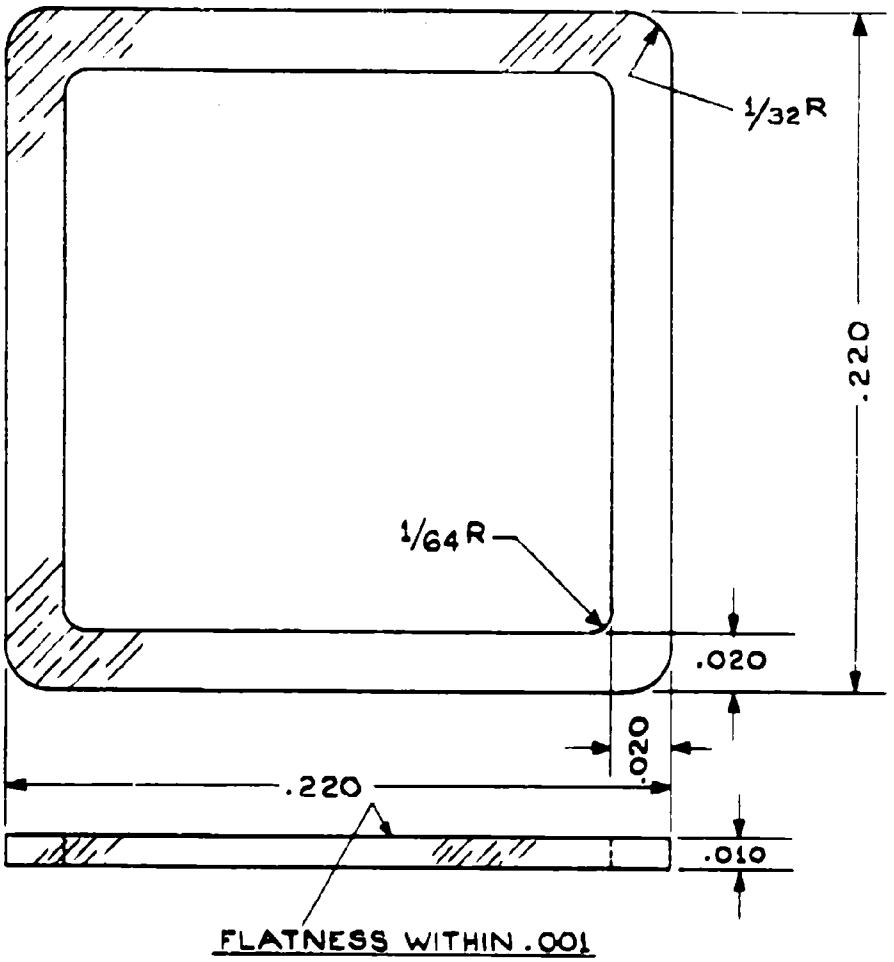
TITLE GLASS PREFORM

291A844

SEMICONDUCTOR DEPT. YOUNGWOOD, PA., U.S.A.

FORM 32725

S.O.	SUB.
D.	1



NOTE:

MAX. BURR AFTER ETCH .0005

ALL DECIMAL DIMENSIONS TO BE WITHIN ±.002

STANDARD TOLERANCES UNLESS OTHERWISE SPECIFIED	
DECIMAL DIMENSIONS	±.003
FRACTIONS	±1/64
ANGLES	±1°

WESTINGHOUSE ELECTRIC CORPORATION

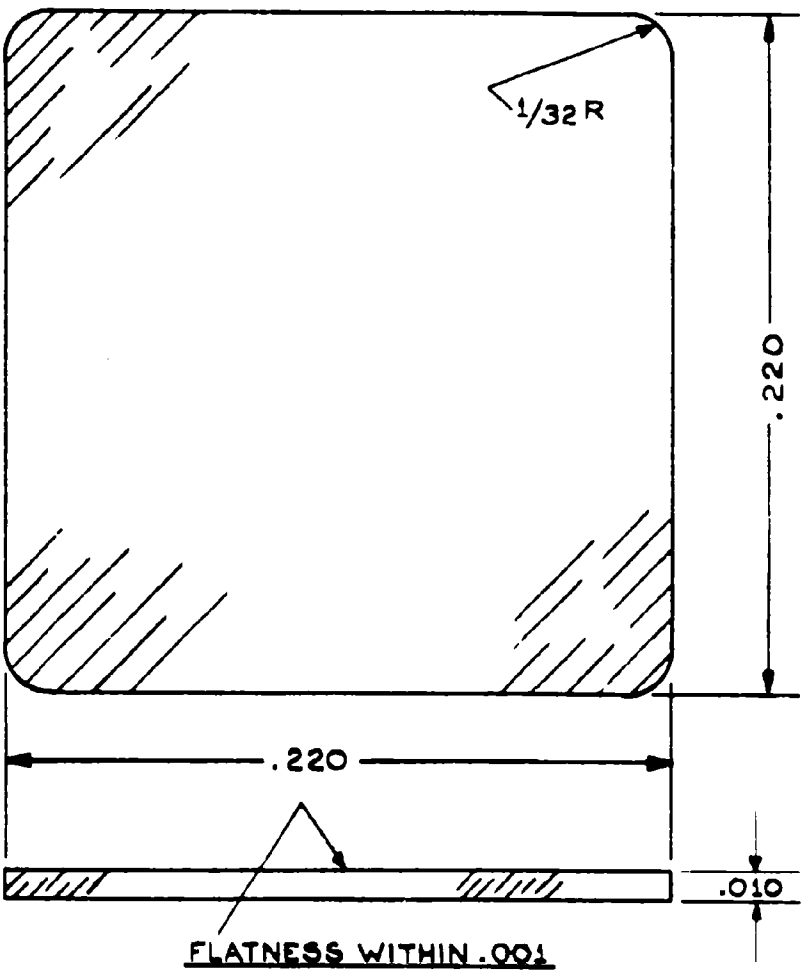
TITLE KOVAR FRAME

291A842

SEMICONDUCTOR DEPT. YOUNGWOOD, PA., U.S.A.

FORM 32723

S.O.	SUB.
D.	1
6P[illegible]	[illegible]



NOTE:

MAX. BURR - .0005

ALL DECIMAL DIMENSIONS TO BE WITHIN .002

STANDARD TOLERANCES UNLESS OTHERWISE SPECIFIED	
DECIMAL DIMENSIONS	±.005
FRACTIONS	±1/64
ANGLES	±1°

WESTINGHOUSE ELECTRIC CORPORATION

TITLE KOVAR LID AND BOTTOM

291A845

SEMICONDUCTOR DEPT. YOUNGWOOD, PA. U.S.A.

FORM 32725

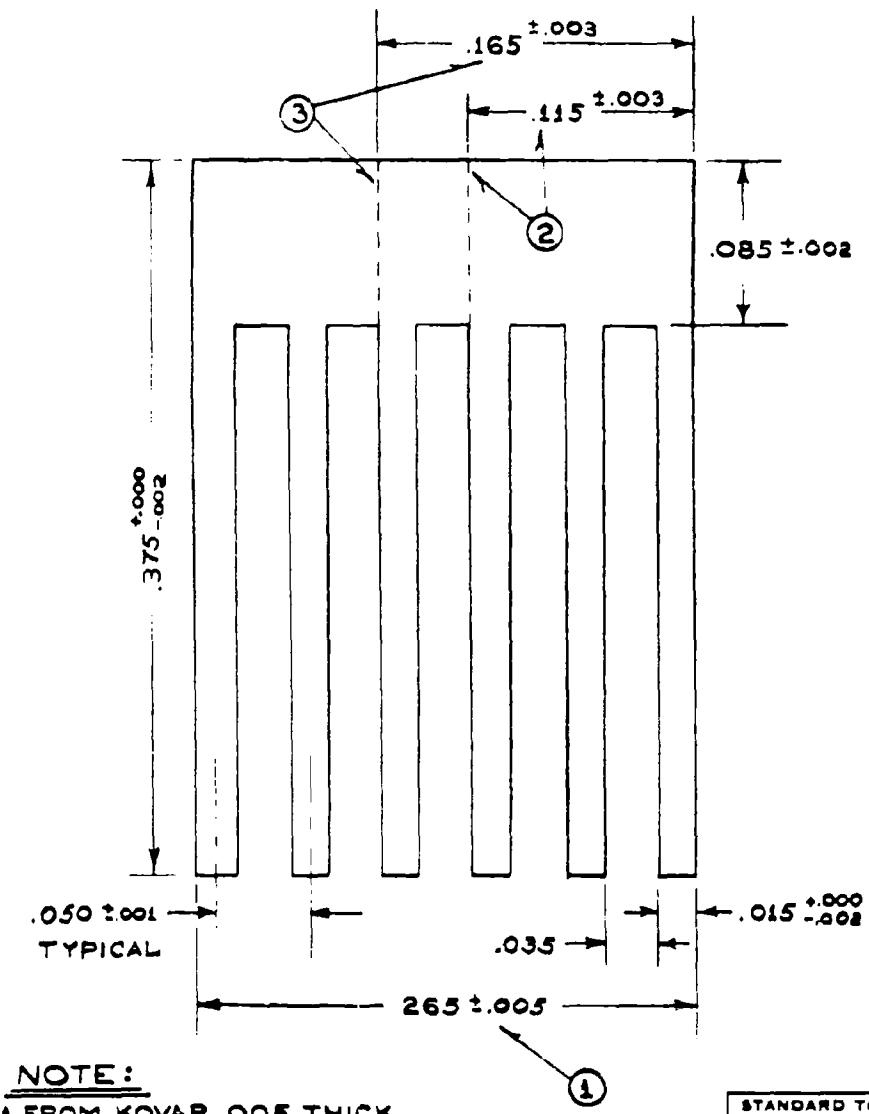
1106A39H02

S.O.	SUB.	SYM.	ITEM	DESCRIPTION	STYLE NO.	
D. 3/21/62	1		1	LEAD PREFORM KOVAR	1106A39H01	
3/21/62			2	LEAD PREFORM KOVAR	1106A39H02	PREFORM CUT AS SHOWN.
			3	LEAD PREFORM KOVAR	1106A39H03	PREFORM CUT AS SHOWN

PS
1106
[illegible]

2

ADDED NOTES
2&3
D Z. 2-25-63
[illegible]



NOTE:
1 FROM KOVAR .005 THICK.
2 MAX. BURR .0005 AFTER ETCH.
3 PACKAGE TO MINIMIZE BENDING OF LEAD PREFORMS.

STANDARD TOLERANCES UNLESS OTHERWISE SPECIFIED	
DECIMAL DIMENSIONS	±.003
FRACTIONS	±1/64
ANGLES	±1°

WESTINGHOUSE ELECTRIC CORPORATION

TITLE LEAD PREFORM (SUPERCEDES DWG. A291262)

1106 A39

SEMICONDUCTOR DEPT. YOUNGWOOD, PA., U.S.A.

FORM 32725

2.3 Package Fabrication

Component parts of the microminiature integrated circuit package are processed as shown in Figure 3. Kovar leads, frames and bottoms are ultrasonically degreased at room temperature in an organic solvent and oxidized at 700°C prior to assembly into package structure. Glass preforms were ultrasonically degreased and cleaned in hydrofluoric acid at room temperature. The package design shown in Exhibit 1 was hermetically sealed in a graphite boat at approximately 950°C in a conveyor type furnace under a nitrogen atmosphere. After sealing the packages are sand-blasted, degreased, deoxidized and finally gold plated.

2.4 Process Problems

The usual difficulties that accompany the development of any product had to be overcome. These are listed below with the respective solution that was applied.

2.4-A Package Mechanical Dimensions

The frame of the package was disoriented with respect to the base. This was primarily due to a 4° drift on the cavity of the glassing boat. The purpose of drift is for ease in package removal. However, this allowance in addition to tolerance clearances due to part variation permitted up to .015 skewing of base to frame. The glassing boats were redesigned. The outside cavity walls which orient the frame to the base have no drift. Also, the clearance

PEB PACKAGE FLOW CHART

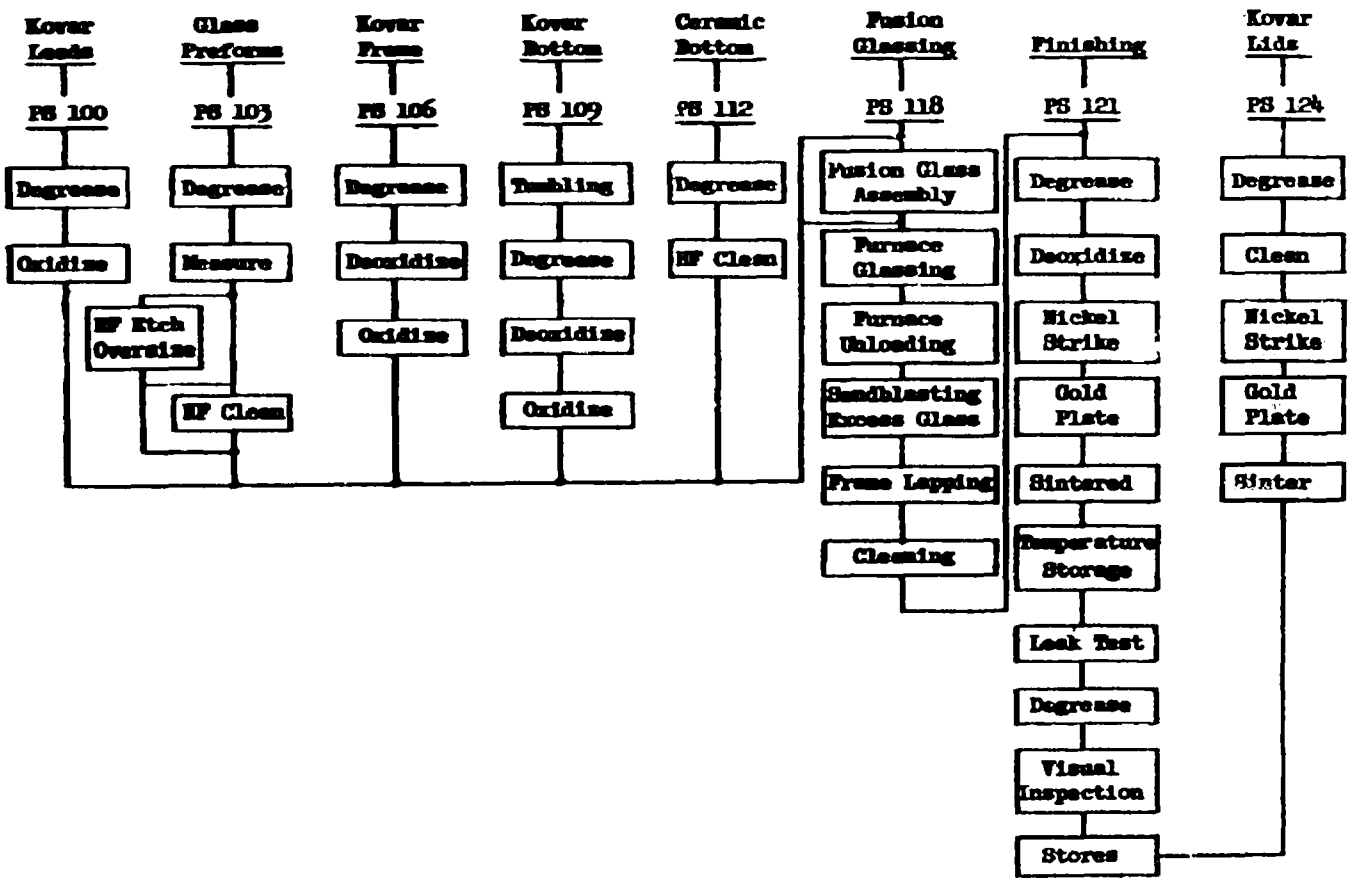


FIGURE 3

2.4-A Package Mechanical Dimensions (contd.)

was reduced in half. This was possible due to the ability of the boat supplier to hold ± .002 tolerance. See Figure 4. Also, the height of the alignment top was reduced which resulted in ease of assembly and more assurance that all parts were properly seated. These changes worked very well resulting in more uniformity in the package as the alignment top and outside retaining walls held all parts in orientation.

2.4-B Physical Shorts

During the glassing operation, the multiform glass preform becomes molten. It flows into the cavity and becomes attached to the oxided frame. With proper boat designs and furnace cycle combinations, the frame and leads maintain a spacing inherent in the boat design. However, in early pilot runs, the frame was lifting and touching the lead preform. This condition is an electrical short between the leads and the frame. This problem was eliminated by a slower heat-up cycle during the glassing operation. It was the writer's opinion that the glass softens and reaches an equalibrium condition rather than a rapid melting which changes the physical location of the glass before surface tension is minimized. As a result of this change, shorting between the leads and frame is almost nonexistent. In fact, all packages are tested at 200 V_{DC} between the leads, frame and base with no noticeable leakage. See Figure 5 for test fixture sketch.

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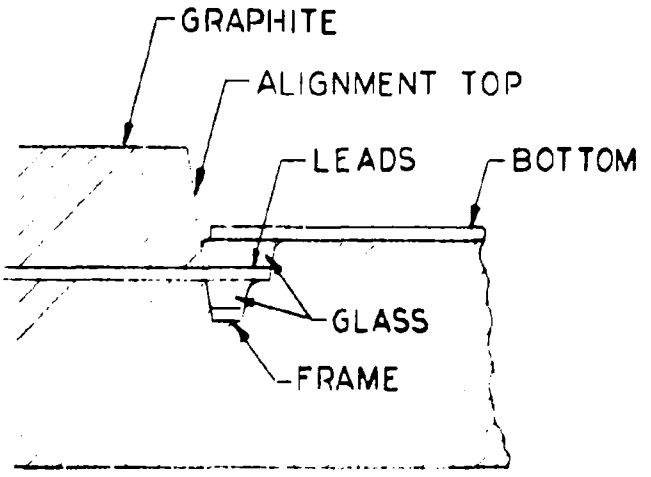
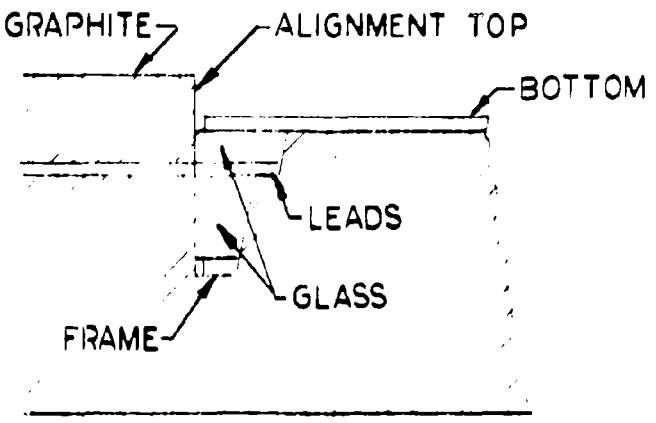


OLD DESIGN



NEW DESIGN

FIGURE 4

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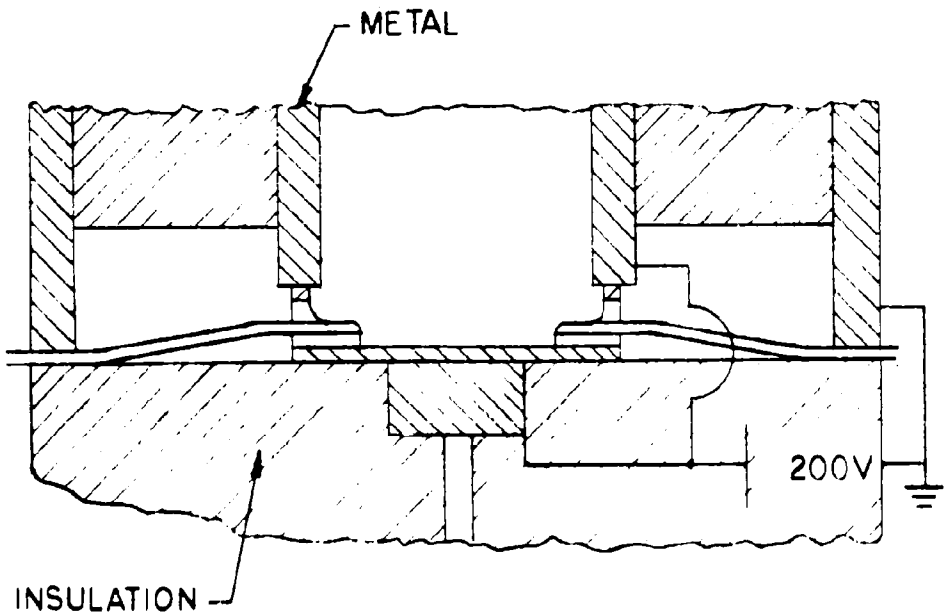


HIGH POTENTIAL BREAKDOWN TEST FIXTURE

FIGURE 5

2.4-C Pitted Kovar from Deoxidizing Process

After package fabrication, the kovar parts have a heavy oxide which would hinder gold plating. This oxide is removed by cleaning in a solution of ferric ammonium sulfate, sulfuric and hydrochloric acid. The solution is quite effective in that all the oxide is removed. However, the cleaning solution leaves the metal parts in a pitted condition. This requires extreme care in etching so that pitting depth is kept to a minimum; since deep etch pits could act as stress centers in bending and result in breakage of leads during fatigue test. As a result of this problem, various deoxidizing solutions were investigated. One of the more promising cleaning solutions was 50% HCL etching at room temperature for ten (10) minutes. This resulted in considerably less pitting of the kovar parts. See photographs 1 and 2.

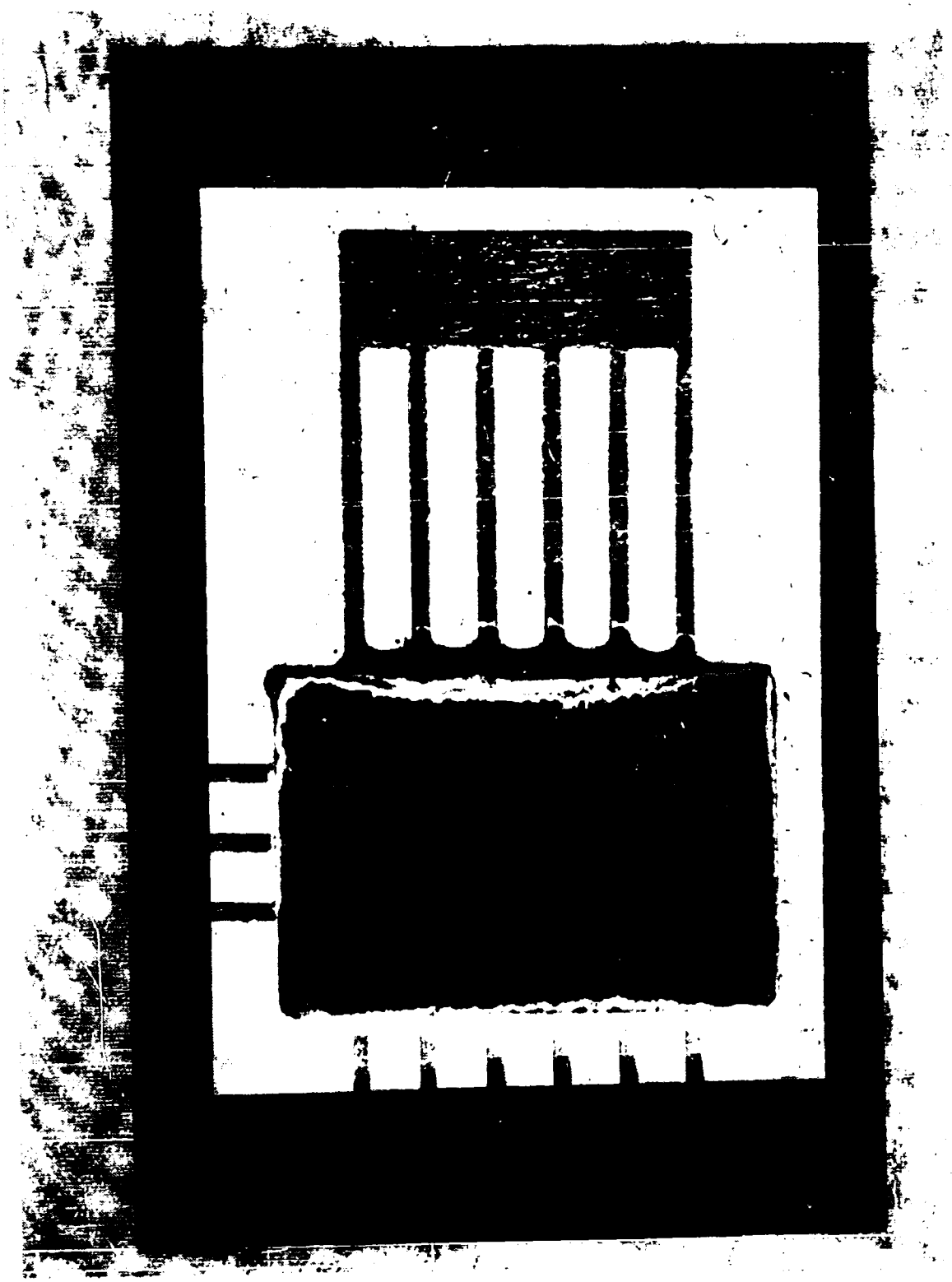
2.4-D Stamped Lead Preforms

Lead preforms which were furnished in the first 100 samples were etched by the photoresist process. This resulted in an undercut lead which appears as a trapezoid. See Figure Nos. 6 and 7. The stamped lead is more uniform in cross section. This is very important in lead fatigue. The etched lead with the trapezoid structure will result in more stress during bending than the stamped lead.

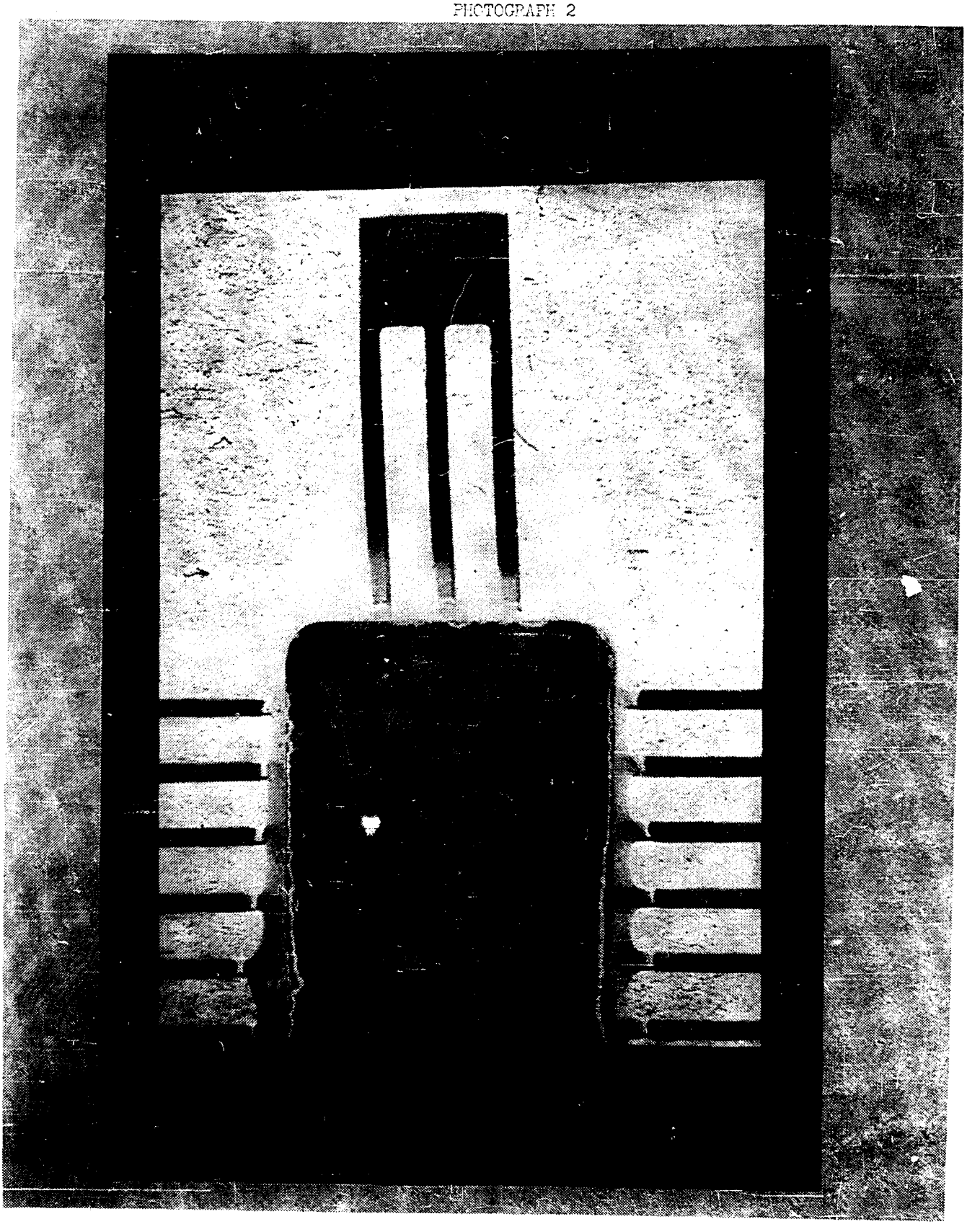
2.4-E Lidding Technique for Microminiature Circuit Packages

A technique for sealing lids on the package was developed during the second quarter of this contract. The packages were sealed in

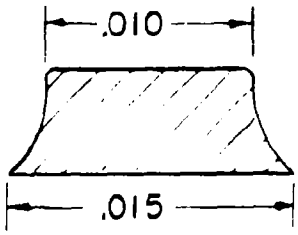
PHOTOGRAPH 1



PHOTOGRAPH 2

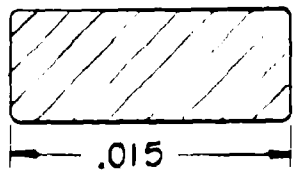


WESTINGHOUSE ELECTRIC CORPORATION



CROSS SECTION OF ETCHED LEAD

FIGURE 6



CROSS SECTION OF STAMPED LEAD

FIGURE 7

2.4-E Lidding Technique for Microminiature Circuit Packages (contd.) a nonoxidizing atmosphere in a continuous belt furnace. Many fixture innovations were tried as the sealing objective is not to melt gold germanium eutectic on the bottom of the package and have complete flow of this same solder between the lid and frame. A differential of 15°C was obtained utilizing a spring with high contact pressure, but low heat inertia, and a graphite boat for positive location of the lid to the package. See Figure 8 for suggested lidding boat. Results in sealing were very encouraging. For all practical purposes, the lidding yield was 100%. The sealed packages were placed in a helium backfill chamber at two (2) atmospheres of pressure for a period of two (2) hours. After which they were helium-leak tested within fifteen (15) minutes and results indicated that they were 1×10^{-7} cc/sec. at one (1) atmosphere in lead rate. These same sealed packages were tested to check for gross leakers in water at 90°C.

The braze used was gold germanium obtained from Automation Alloys with a melting point of 352°C. Packages of another size were stored with no resulting leaks or physical change in the package at 300°C for 1000 hours. Fifty .220 x .220 integrated circuit micromodule packages were sealed in the aforementioned manner and submitted for Signal Corps evaluation.

2.5 Comparison of Helium Leak Test Versus RADIFLO Leak Test Measurement

In order to determine the accuracy of our helium leak test technique, an experiment was set up to cross check our present technique versus

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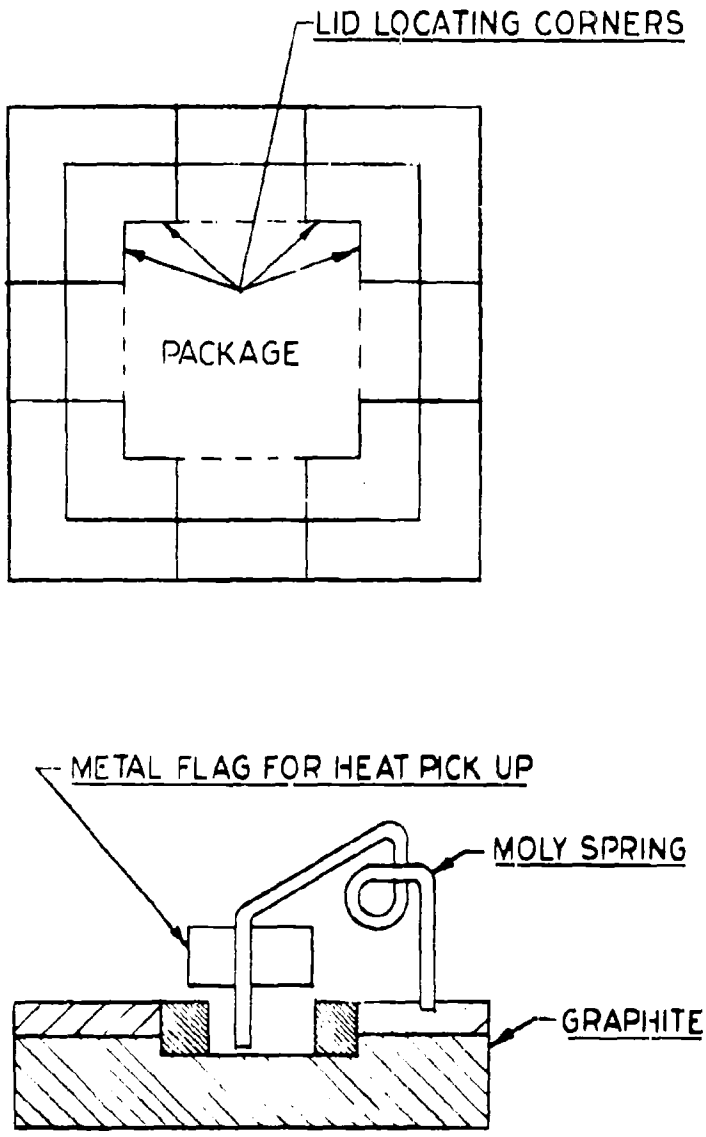

FIGURE 8

2.5 Comparison of Helium Leak Test Versus RADIFLO Leak Test Measurement (contd.)

RADIFLO leak testing. The latter is a quantitative method of measurement.

Seventy-seven packages or 26 lidding boats of packages were sealed in the standard production equipment. After sealing the packages were gross leak tested. This is conducted by immersing the package in a 90°C alconox (wetting agent) water solution for 15 seconds and observing for continued bubble formation. These are rejected as gross leakers. In this group no packages were rejected. The unusual number of 77 to be sealed was a result of 100 package starts from initial fabrication. Our typical losses on gross leak test are less than one per cent. After gross leak checking, the packages are placed in a pressure chamber. The chamber is evacuated for a minimum of 30 minutes, then pressurized for a minimum of two hours at four atmospheres of helium. The packages were removed and blown off with compressed air to remove adherent helium molecules from their surface. The packages were then helium leak tested using a CEC leak detector. The equipment was calibrated at two levels to insure proper operation over the test range of equipment prior to commencing test.

The test results of these 77 sealed packages had the following distribution:

Leak Rate	Number
$<1 \times 10^{-6}$ $\geq 1 \times 10^{-7}$	6
$<1 \times 10^{-7}$ $\geq 1 \times 10^{-8}$	8
$<1 \times 10^{-8}$ $\geq 1 \times 10^{-9}$	10
$<1 \times 10^{-9}$ $\geq 1 \times 10^{-11}$	9
No detectable leaks	44

2.5 Comparison of Helium Leak Test Versus RADIFLO Leak Test Measurement (contd.)

Identity of each package was maintained and forwarded to Consolidated Electro Dynamics Corporation for RADIFLO measurements on the packages. The RADIFLO technique uses radioactive krypton and is considered to be a quantitative measuring technique since an actual count of the radioactive ions that diffuse into the package are measured. Whereas, the helium bomb method only measures the amount of helium that escapes the interior of the package. Since this percentage is variable and subject to wide variations, helium bomb test procedure is only a qualitative means for measurement. The results of the RADIFLO comparison proved this hypothesis as shown below:

		Helium	RADIFLO
Number Tested		77	77
Detectable Leaks		33	12
Specific Readings	#7	2×10^{-7} cc/sec	2×10^{-8} cc/sec
	#11	7×10^{-8} cc/sec	2×10^{-9} cc/sec
	#22	3×10^{-7} cc/sec	1×10^{-9} cc/sec

The higher leak rate measured by the helium leak test method is primarily due to incomplete removal of absorbed helium on the surface. The RADIFLO measurements are within 20% as the results are based on constant volume as this is the volume tolerance of the integrated circuit package.

2.6 Microminiature Integral Circuit Models

Twenty-four Westinghouse Functional Electronic Blocks were encapsulated in the .225" x .225" x .045" microminiature integrated circuit package. These blocks were selected at random from the Universal RF Amplifier product line. The FEB circuits were wafer bonded to the kovar bottom of the package using a gold alloy preform. The operation

2.6 Microminiature Integral Circuit Models (contd.)

was accomplished in a nitrogen atmosphere on a 425°C strip heater. After wafer bonding, lead were attached to the circuit pads and to their respective terminals. The Universal RF Amplifier was .060" x .060" square and is shown in Figure 9. The leads were attached with a standard K & S Model 447 nail head bonder with a modified heat column top to suit package structure. The lead attachment operation was accomplished in approximately 20% less time than our standard .250" x .250" package with leads on two sides. This was due primarily to shorter distance between leads and pads. This results in shorter wire length and less clearance problems caused by leads crowding. Lidding was performed in a conveyorized electric furnace at 365°C utilizing gold germanium eutectic preforms. Encapsulation yields achieved were in excess of 90%. Devices were electrically tested and placed in proper categories. See Figure 10 showing test data. These were grouped into four device types, Video, IF, Oscillator-Mixer and RF, of six each. Two detectors and six audio amplifiers were also encapsulated. Two 10.3 Mc quartz crystals and eight 455Kc IF filters were secured. Ninety empty sealed packages were also processed. These items were furnished as working models of the microminiature integrated circuit packages.

2.7 Microminiature Circuit Package Production

These packages were scheduled into our manufacturing over a four month period. Production was interrupted in late July and August due to the transfer of the package activity to the new Molecular Electronics Division Site in Elkridge, Maryland. No major problems

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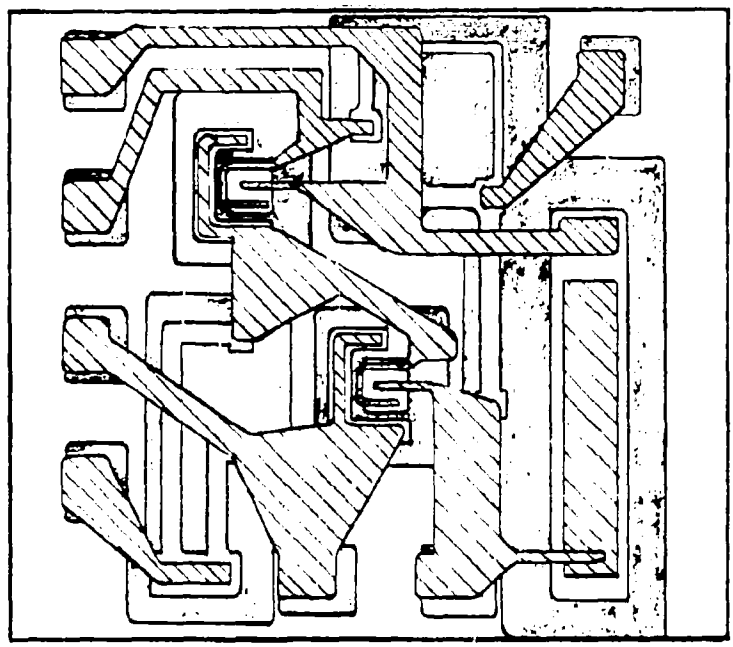


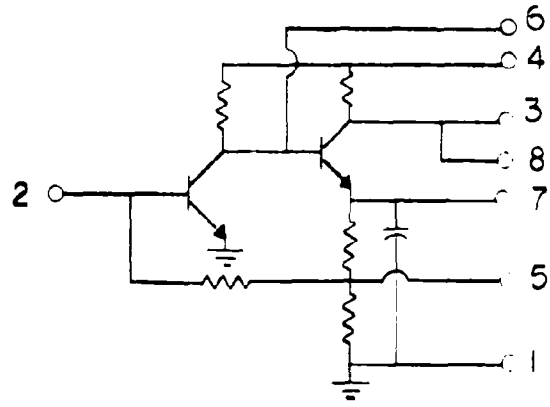


FIGURE 9

UNIT	CURRENT DRAIN	INSERTION GAIN PIN 3 @ 10.7 MC	INSERTION GAIN PIN 3 @ 455 KC	INSERTION GAIN PIN 3 @ 3.2 MC	INSERTION GAIN PIN 3 @ 455 KC	POSSIBLE FUNCTION	FREQ. CUT-OFF FROM 455 KC REF. PIN 3 OR PIN 7	FUNCTION	MAX. OUTPUT VOLTAGE NO LOAD PIN 3 OR PIN 7	MAX. OUTPUT VOLTAGE LOAD	INPUT IMPEDANCE @ 455 KC PIN 3 OR PIN 7	OUTPUT IMPEDANCE @ 455 KC PIN 3 OR PIN 7	CONVERSION GAIN 10.7 MC	ROUTE
	MA	db	db	db	db		MC		V	V	Ω	Ω	db	
Video - [illegible]1106														
00002	3.0	20.1	34.0	40.0	43.5	V	18.0	V	1.2	.15	205	1.5K	29	G-18
00009	3.2	20.2	34.2	39.5	40.0	V	18.0	V	1.2	.16	190	1.27K	28	G-18
00017	3.4	20.0	34.0	39.0	42.2	V	15.5	V	1.2	.15	200	1.3K	27	G-18
00020	3.0	20.0	34.5	40.2	42.5	V	18.0	V	1.2	.15	236	1.4K	275	G-18
00034	2.9	20.0	34.0	38.5	43.0	V	14.4	V	1.2	.14	244	1.25K	28	G-18
00045	3.0	20.0	34.1	40.0	43.9	V	15.0	V	1.4	.15	233	1.35K	28	G-18
I.F. - [illegible]1103														
00004	3.4	20.0	21.2	31.0	41.0	V	6.0	IF	1.2	.15	250	200		G-24
00006	3.1	19.1	22.0	30.0	41.5	IF	10.2	IF	2.0	.56	353	110		G-24
00007	3.4	20.0	21.0	30.0	41.2	V	15.0	IF	1.1	.15	231	190		G-24
00005	2.9	19.0	33.9	35.0	40.0	IF	2.65	IF	1.0	.74	595	120		
00024	3.0	20.0	34.0	36.5	41.9	V	9.0	IF	1.3	.14	254	205		G-24
00026	2.9	19.0	32.3	32.3	37.5	IF	2.75	IF	2.2	.9	59	130		G-24
00037	2.9	19.0	34.0	35.3	40.5	IF	2.7	IF	2.2	.6	428	122		G-24

FIGURE 10

UNIT	CURRENT DRAIN MA	INSERTION GAIN PIN 3 @ 6 MC db	INSERTION GAIN PIN 3 @ 455 KC db	INSERTION GAIN PIN 3 @ 3 MC db	INSERTION GAIN PIN 3 @ 455 KC db	POSSIBLE FUNCTION	FREQ. CUT-OFF FROM 455 KC REF. PIN 3 OR PIN 7 KC	FUNCTION	MAX. OUTPUT VOLTAGE NO LOAD PIN 3 OR PIN 7 V	MAX. OUTPUT VOLTAGE LOAD V	INPUT IMPEDANCE @ 455 KC PIN 3 OR PIN 7 Ω	OUTPUT IMPEDANCE @ 455 KC PIN 3 OR PIN 7 Ω	CONVERSION GAIN 10-30 MC db	ROUTE
ac. Mixer M1102														
09896	3.0	18.5	20.0	33.0	36.2	FF	10.2	O.I.	2.2	.72	698	125	24	G-20
09899	3.1	19.0	20.0	39.0	41.5	FF	11.0	O.I.	2.5	.7	565	140	24	G-20
09903	3.0	20.0	35.0	39.0	43.0	V	15.0	O.I.	1.2	.13	65.8	75	27	G-20
09914	3.4	18.0	32.0	31.5	39.5	FF	3.5	O.I.	2.3	.21	247	150	20	G-20
09938	2.8	20.0	34.5	36.5	41.5	V	20.0	O.I.	1.1	.14	316	90	24	G-20
09941	3.0	20.0	34.0	36.3	42.0	V	10.0	O.I.	1.2	.15	298	170	26	G-20
R.F. - M1101														
09895	3.5	20.5	21.5	39.1	41.5	V	6.5	FF	1.2	.3	209	225	27	G-22
09911	3.3	20.0	34.0	40.0	42.5	V	13.6	FF	1.2	.3	189	200	28	G-22
09913	3.0	20.0	34.2	39.0	42.5	V		FF	1.2	.15	154	190	22	G-22
09925	3.1	20.0	34.6	34.0	43.0	V	2.9	FF	1.2	.15	154	190	22	G-22
09935	3.2	20.0	34.0	38.0	43.0	V	13.0	FF	1.2	.15	220	200	27	G-22
09943	2.6	18.0	34.0	30.0	40.5	FF	2.6	FF	2.0	.55	79	180	28	G-22

FIGURE 10

2.7 Microminiature Circuit Package Production (contd.)

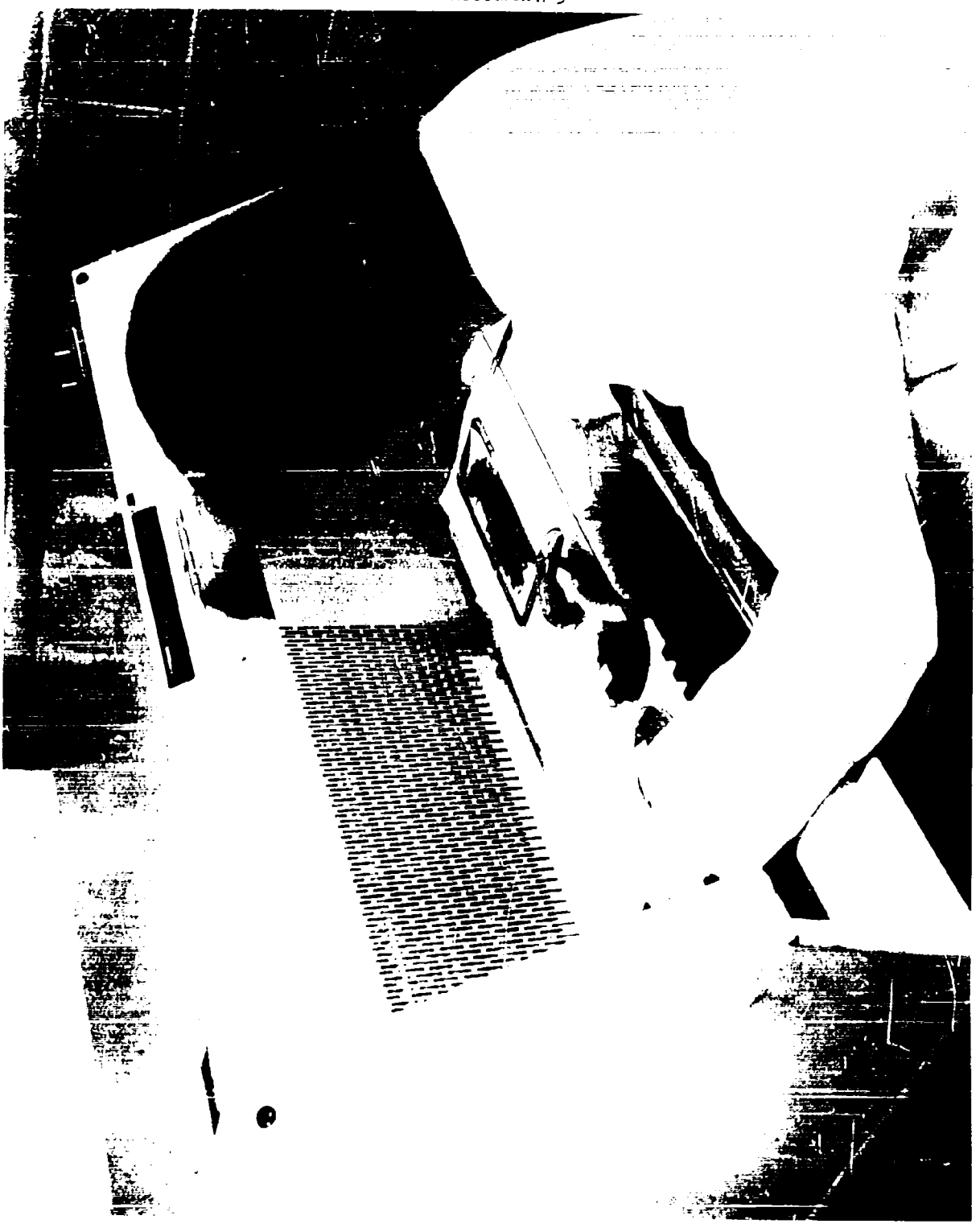
were encountered and product yields were comparable to our standard Westinghouse Flat-Paks. Ninety per cent of the unsealed packages measured were 1×10^{-8} cc/sec leak rate of helium at one atmosphere.

A review of the process steps with some photographs may give a better insight to the processes utilized.

Kovar material is oxidized in a batch operation and forwarded to the assembly area. The glass preforms are hydrofluoric etched and also forwarded to the assembly area.

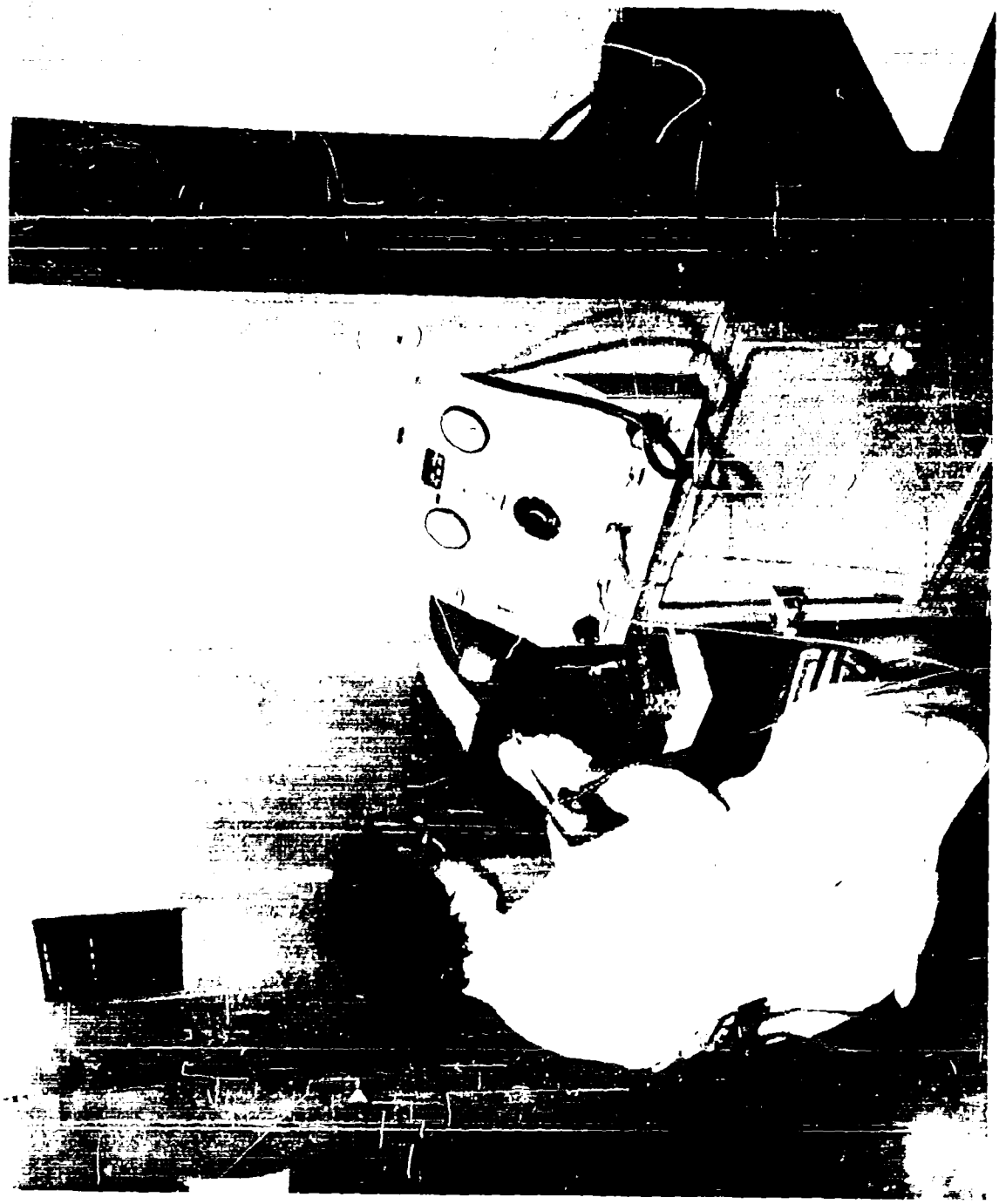
At this location frames, leads, glass, kovar bottoms and weights are loaded in that order into glassing boats. See photograph 3 which illustrates the assembly of the microminiature circuit package. After sealing the packages are unloaded from the glassing boat. In the sealing operation the packages are joined both mechanically and hermetically through the glass to metal oxide bond. See photograph 4 showing the unloading of packages. After unloading it is necessary to blast of a light film of glass which may form on the oxide leads and bottom. This operation is accomplished with a White abrasive machine. See photograph 5 for sandblast operation. After the excess glass is removed from the terminals and pad, it is necessary to remove glass from the top surface of the frame. This operation is accomplished on a rotary lapping machine. See photograph 6 for lapping operation. After lapping the surface is deoxidized and gold plated in a batch operation. After these operations the packages are inspected physically 100% for mechanical defects. See photograph 7 for inspection

PHOTOGRAPH 3



PHOTOGRAPH 4

PHOTOGRAPH 5



PHOTOGRAPH 6

PHOTOGRAPH 7

PHOTOGRAPH 8

2.7 Microminiature Circuit Package Production (contd.)

station. After mechanical inspection packages are helium leak tested 100%. This operation can be seen on photograph 8.

2.8 Encapsulation Procedures for Microminiature Circuit Packages

The following data is presented as suggested techniques for encapsulating circuits in the microminiature circuit packages. Undoubtedly, high volume techniques could be developed over these presented, but following these procedures will typically yield 95% of device encapsulation starts.

2.8-A Cleaning of Packages, Circuits & Gold Preforms Prior to Wafer Bonding

1. Immerse the parts in hot TCE for three minutes. Using fresh TCE with every cleaning batch.

2. Immerse the degreased parts in hot acetone for three minutes pour off solvent and repeat this step. Remove parts and dry under a heat lamp.

3. Store parts in sealed containers prior to use.

2.8-B Circuit Mounting in Microcircuit Packages

1. Place microcircuit package on strip heater using spring hold down to maintain good thermal contact. Design fixture so that entire package is flooded with inert atmosphere such as nitrogen.

2. Place gold preform and integrated circuit on package at desired locations. Grasp silicon chip at the edges with sharp tweezers. Apply downward pressure until gold preform melts as exhibited by

2.8-B Circuit Mounting in Microcircuit Packages (contd.)

flow at the circuit periphery. At this time, move circuit in a scrubbing motion to firmly seal the circuit and to obtain a sound metallurgical joint.

3. Remove package and place in closed container for lead attachment operation.

2.8-C Lead Attachment of Integrated Circuit to Microcircuit Package

1. Place microcircuit package in heat column fixture. The fixture should be designed to use spring loading applying pressure to the package frame for good thermal contact. Spring loading should also be applied to the terminals to raise the temperature of the terminals to raise the temperature of the terminals to bonding temperature. Approximately 250 to 300°C depending on bonding capillary loading. The fixture should provide proper inert gas flow over the package to prevent oxidation. External leads should be shielded from flame-off if nail head bonding is used.

2. Either wedge or nail head bonds can be made to the terminals. Bond times can be less than two seconds duration when weight and terminal temperatures are properly adjusted.

3. Check quality of bond by attaching wire to package leads and remove connection with tweezers. If bond attachment is proper, wire will break prior to any disturbance of lead joint. If bond pulls loose, check package cleanliness, bond temperatures, gold plating quality or wire material.

2.8-D Lid Attachment of Microcircuit Package

1. Rinse assembled microcircuit package, gold germanium preforms, and gold plated kovar lid in ultra pure methanol. Dry under heat lamp and vacuum bake at 1×10^{-3} mm of Hg. for one hour at 175°C. Store baked parts in a closed container.

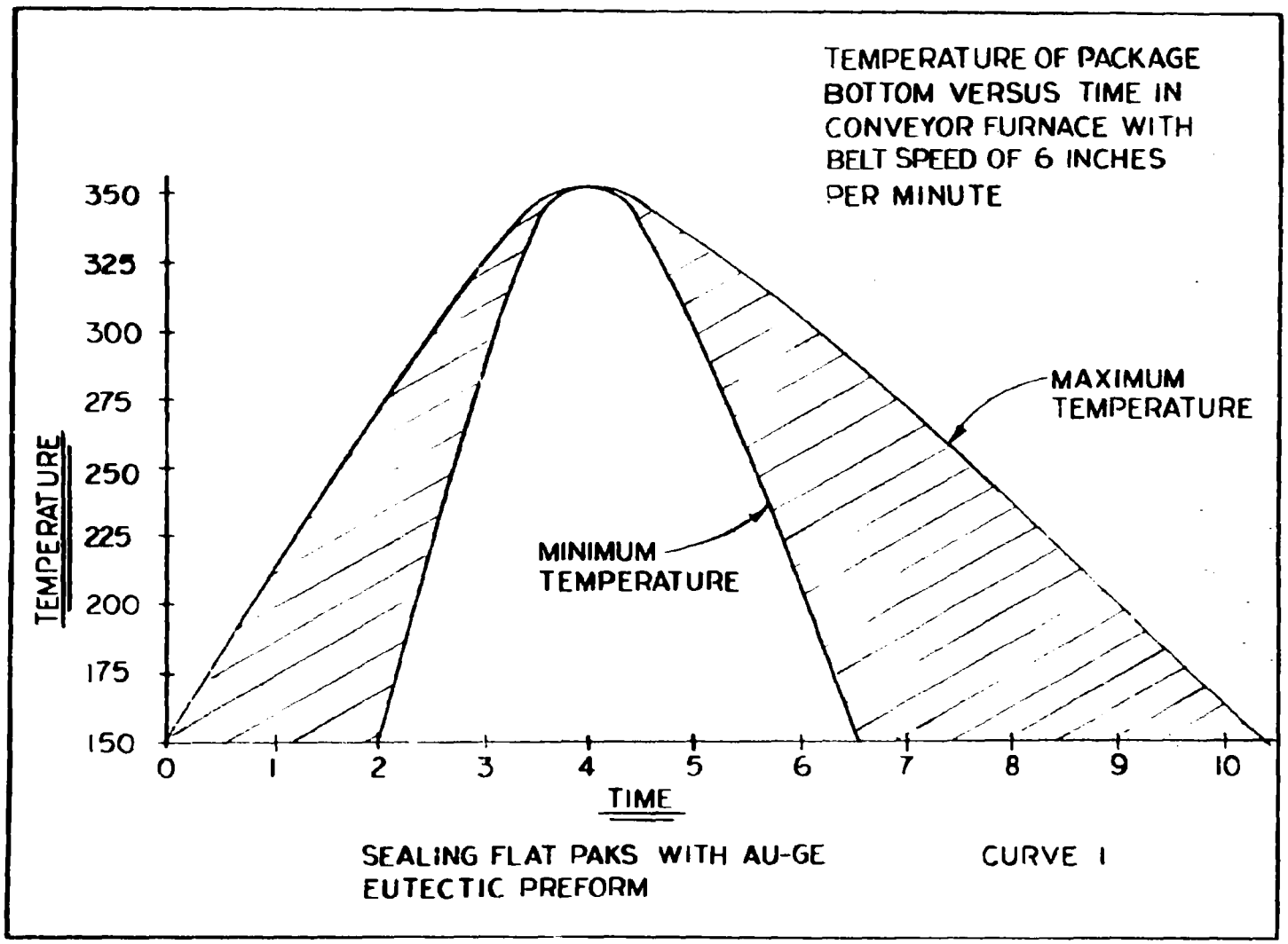
2. Assemble package, preform and lid into graphite fixture. The fixture contacts the lid only at corners to fix orientation. The fixture uses a heavy spring with approximately 100 grams loading applied to the lid. This design is conducive to higher temperature on the lid and the package bottom at least 10°C lower due to the mass of the graphite fixture.

3. Load the fixture onto the conveyorized belt furnace. The equipment is an electric furnace utilizing either a dry hydrogen or nitrogen atmosphere. The temperature and belt speeds are adjusted to minimize the time at sealing temperature. The most successful time arrived at was one minute at 360°C on the lid. The measured temperature on the device was less than 350°C. See curve 1 illustrating dynamic profile of lidding furnace.

4. The resultant sealed package should be void free and a smooth continuous fillet be apparent at the lid and frame joint.

2.8-E Leak Test Procedure for Sealed Microminiature Packages

1. Leak test for gross leaks by immersing in 90°C alconox water solution for 15 seconds and observe for continued bubble formation. Reject for any apparent leaks.



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2.8-E Leak Test Procedure for Sealed Microminiature Packages (contd.)

2. Helium leak test for finite leaks by loading sealed microcircuit packages in a pressure chamber. Evacuate for a minimum of 30 minutes, backfill for two hours minimum with four atmospheres of helium. Leak test within two hours after blowing off carefully with compressed air. This is necessary to rid the package surfaces of adherent helium. Use standard leak detector such as Vecco or CEC. There should be little or no deterioration over the initial package leak rate after sealing.

III. CONCLUSIONS

The package developed for the Signal Corps Contract No. DA-36-039-SC-90850 is a very workable package. Manufacturing cost of this package was comparable to our standard package line. Environmental data collected on high temperature storage, salt spray, vibration, etc., on similar package structures indicates that this package will meet MIL S19500 requirements.

Hermeticity achieved with the gold germanium seal is excellent and unaffected by high temperature storage or enviornmental testing. The overall strength of the package is good in that leads can be bent several times without fear of breakage or loss of hermeticity. Encapsulation yields of integrated circuits in this package type are in excess of 90% resulting in low overall packaging cost. Also no expensive equipment beyond standard transistor assembly equipment is required. All equipment used in assembling the Westinghouse FEB's in the microminiature integrated circuit package was obtained commercially.

IV. PROGRAM FOR CONTINUED IMPROVEMENT

Although the contract is coming to an end, work will be continued on the microminiature integrated circuit package as it is now part of our standard product line. Several of the major product improvement programs are listed below:

1. Investigation of various lead materials or coatings to eliminate gold plating at wire bond points.

2. Evaluation of new gold plating techniques to increase oxidation resistance.

3. Improved dimensional control of package through new boat structures.

4. Variations in sealing techniques to minimize circuit temperatures.

V. KEY TECHNICAL PERSONNEL

The following key personnel were assigned to the project during this report period:

E. P. Barbaro	Manager	600 Hours (Not charged to project.)
T. L. Charland	Senior Engineer	405 Hours
J. M. Clayton	Associate Engineer	155 Hours
Others	Technicians	5000 Hours
Total Hours Charged to Project		5560 Hours

The background of each key technical person is contained on the following separate pages.

BARBARO, ERNEST P.
Supervising Engineer, Pilot Manufacturing
Molecular Electronics Division

Born: August 21, 1929
Married: Three Children

Education:

University of Pittsburgh, B.S. in Industrial Engineering, M.E. Option, June 1951

University of Pittsburgh, M.S. in Engineering, August 1957

Experience:

July 1951 – July 1953: General Motors Corp., Dayton, Ohio - Process and Design Engineer, Delco Products - Responsible for Design, Installation of Process Equipment.

July 1953 – August 1956: Westinghouse Electric Corp. - Materials Division Penn Avenue, Pittsburgh, Pa. - Assistant Engineer. Responsible for miniature selenium rectifier process and design. Designed and supervised environmental test facility. Developed automatic test equipment for basic cells and final assemblies. Mechanized assemblies of miniature selenium rectifiers. Developed high voltage stack, computor diodes, and assisted in the development of high current density selenium cells.

August 1956 – July 1958: Westinghouse Electric Corp. - Director Systems, Penn Avenue, Pittsburgh, Pa. - Supervising Manufacturing Engineer. Responsible for processing, assembly, test, quality assurance, and applications of the manufacturing of selenium rectifiers.

July 1958 – January 1959: Westinghouse Electric Corp. - Semiconductor Dept. Youngwood, Pa. - Manufacturing Engineer

Assigned to take process of 150 watt silicon transistor from pilot to volume manufacture. Worked with Engineering to redesign unit to lower product cost and increase reliability. Work was in areas of alloy development, gold plating process development, connector design, process assembly techniques, welding, painting and testing of the product.

January 1959 May 1962	Westinghouse Electric Corp. - Semiconductor Division, Youngwood, Pa. - Supervising Engineer.

Responsible for product yield and quality improvement for silicon transistors and trinistors, directed large cost reduction program for all control products. Responsible for facility specification. Group contributed significantly to product improvement in the areas of diffusion, alloying, surface passivation, encapsulation design and test techniques.

May 1962 to Present	Westinghouse Electric Corp. - Molecular Electronics Division - Supervising Engineer.

Responsible for assembly and encapsulation of functional electronic blocks. Also, responsible for flat package design and fabrication. Responsible for push-pull amplifier engineering and processing.

Societies:

A.I.E.E.
E.C.S.

Patent Disclosures: 15

Patents: 3

Publications: A New Application of Linear Programming

CHARLAND, TELESPHORE LAWRENCE
Senior Design Engineer
Molecular Electronics Division

Born: March 31, 1921 - Keeseville, New York

Education:

1946-1950	Iowa State University, Ames, Iowa - BS in Ceramic Engrg.
1952-1954	Alfred University, Alfred, New York - MS in Ceramic Engrg.

Experience:

1950-1952	Westinghouse, Lamp Division - engineer concerned with quality control and production of fluorescent lamps.
1952-1954	Alfred University - research associate concerned with development of ceramic materials for jet engine and rocket applications.
1954-1956	Phillips Petroleum Co., Oklahoma City - development of drilling fluid materials.
1956-1961	Westinghouse - Materials Engineering - development of nuclear fuel, cermet, insulation and thermoelectric materials.
1961-Present	Westinghouse, Youngwood - development work in rare earth semiconductor materials for thermoelectric applications, piezoelectric materials for I.F. applications and ceramic materials for functional electronic block packaging applications.

Societies:

The American Ceramic Society; The National Institute of Ceramic Engineers; The American Nuclear Society; The New York State Ceramic Association; Keramos; Registered Professional Engineer, Pennsylvania.

Patent Disclosures:

1 - Cermet Compositions; 1 - Nuclear Fuels; 8 - Thermoelectric Materials; 8 - Patent Disclosure Awards; 7 - Patent Application Awards.

Publications:

The Pressure-Carbonization of Carbon Bonded Silicon Carbide - Graphite for Use in Uncooled Rocket Nozzles

The Hot Pressing of Commercial Chrome Ores

Modification of a Ceramic Nuclear Fuel for Improved Thermal Conductivity

Development of Thermoelectric Materials

CLAYTON, JOHN M.
Associate Engineer
Molecular Electronics Division

Born: February 17, 1936

Married

Education:

Carnegie Institute of Technology, BS Metallurgy, 1962

Experience:

March 1959 September 1959	Allegheny Electronic Chemicals Company, Bradford, Pa. Development of crystal growth techniques and crystal characterization and development of "Sailer's etch."
June 1960 June 1962	Westinghouse Semiconductor Division, Youngwood, Pa. Diffusion and alloying of large area devices. Epitaxial growth development.
June 1962 to Present	Westinghouse Molecular Electronics Division, Youngwood, Pa. Assembly and encapsulation of functional electronic blocks.

Professional Societies:

Electrochemical Society
IEEE
American Vacuum Society

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WESTINGHOUSE ELECTRIC CORPORATION

Elkridge, Maryland

MICROMINIATURE INTEGRATED CIRCUIT PACKAGE
By F. P. Barbaro

Final Progress Report, July 1, 1962 to August 1, 1964. Signal Corps Contract No. DA-36-039-SC-90350, DA Project No. 3A99-21-002-01, Unclassified Report.

Design and fabrication of two metal to glass seal microminiature integrated circuit packages were completed. One which utilized the .410 inch square ceramic base as an integral portion of the package and the other a .225 inch square package per the stated requirements of the contract. The .410 inch square package required more development as leak rates of only $<1 \times 10^{-8}$ cc/sec at one atmosphere were achieved. However, on the contract package leak rates $<1 \times 10^{-8}$ cc/sec at one atmosphere were attained. This was accomplished through revisions of graphite molds, glass preform designs, kovar oxide layer control, and sealing techniques.

To prove package feasibility, twenty-four Westinghouse Functional Electronic Blocks were encapsulated in the .225 inch square microminiature planar package. No problems in assembly were encountered.

After approval of mechanical samples and packages with integrated circuits, production of the required 10,000 packages commenced. Environmental studies were conducted on this package type confirming reliability of the package structure. Application data was compiled for circuit mounting, wiring, sealing and hermeticity testing of the microminiature circuit package developed for this contract.

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WESTINGHOUSE ELECTRIC CORPORATION

Elkridge, Maryland

MICROMINIATURE INTEGRATED CIRCUIT PACKAGE
By F. P. Barbaro

Final Progress Report, July 1, 1962 to August 1, 1964. Signal Corps Contract No. DA-36-039-SC-90350, DA Project No. 3A99-21-002-01, Unclassified Report.

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